



# EU Chips Act

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**EC - DG CNECT**

*EU Chips Act –  
Challenges & opportunities  
Warsaw, 4 April 2023*



# The “Chip crisis”

## Impact on industries

### Increasing demand



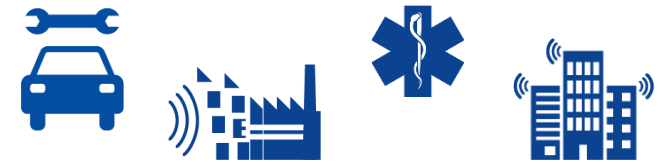
- Accelerated digital transition
- **Increased demand** for semiconductors fueling severe shortage

### Fragile supply chain



- Not resilient to **disruptions** such as COVID-19 pandemic
- **Concentration of production** in Asia (Taiwan, Korea) and high entry costs
- **Geopolitical** tensions (e.g. South China Sea, export control measures)

### Detrimental effects across industries



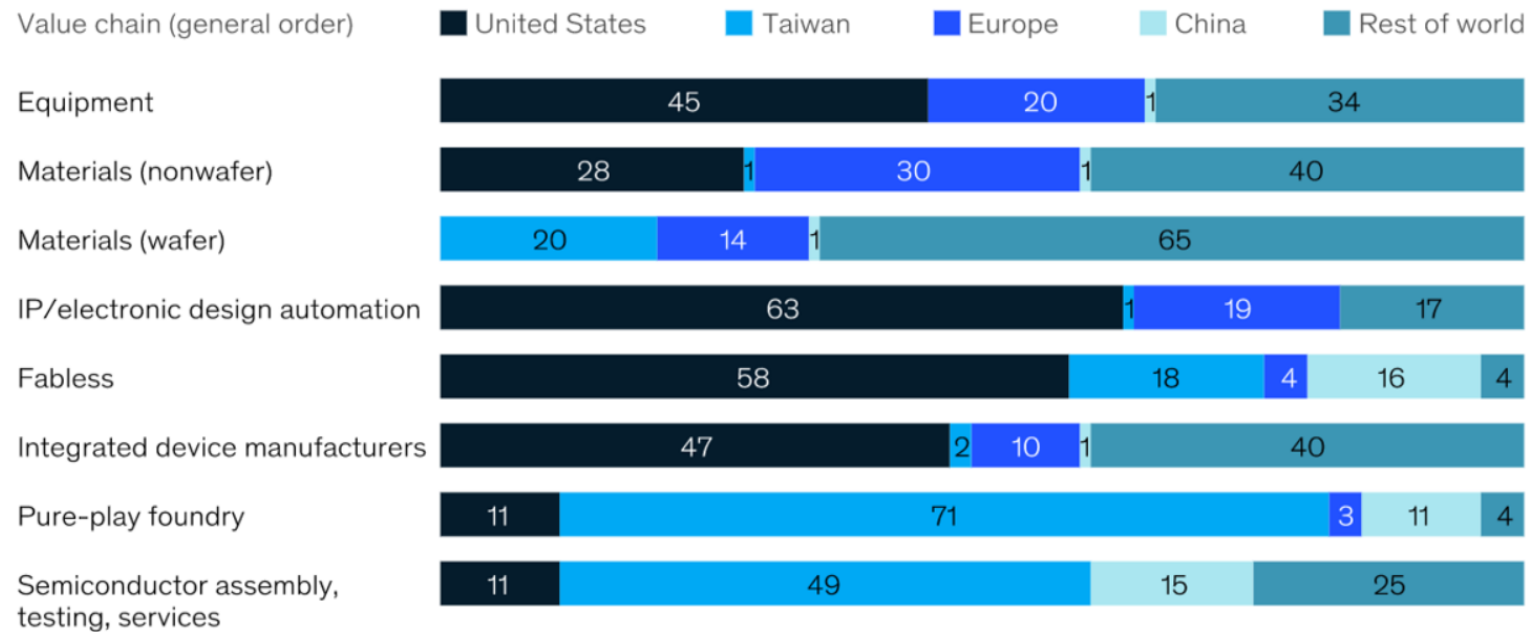
#### *Example: Automotive*

- **11 million less** cars produced in 2021, \$ 210B lost revenues
- **-33%** car sales in Europe

# EU dependencies

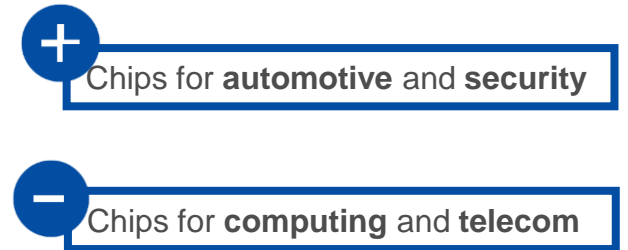
## in chip design, manufacturing and packaging

Value chain



Source: Gartner; IHS; Strategy Analytics; McKinsey

Stage of supply chain	Added value
Chip Design	30%
Semiconductor Manufacturing	34%
Assembly, Test and Packaging	10%



**Investments** in the EU have stagnated and its global market share has fallen below 10%

# Global demand

expected to double and reach USD 1 Trillion before 2030



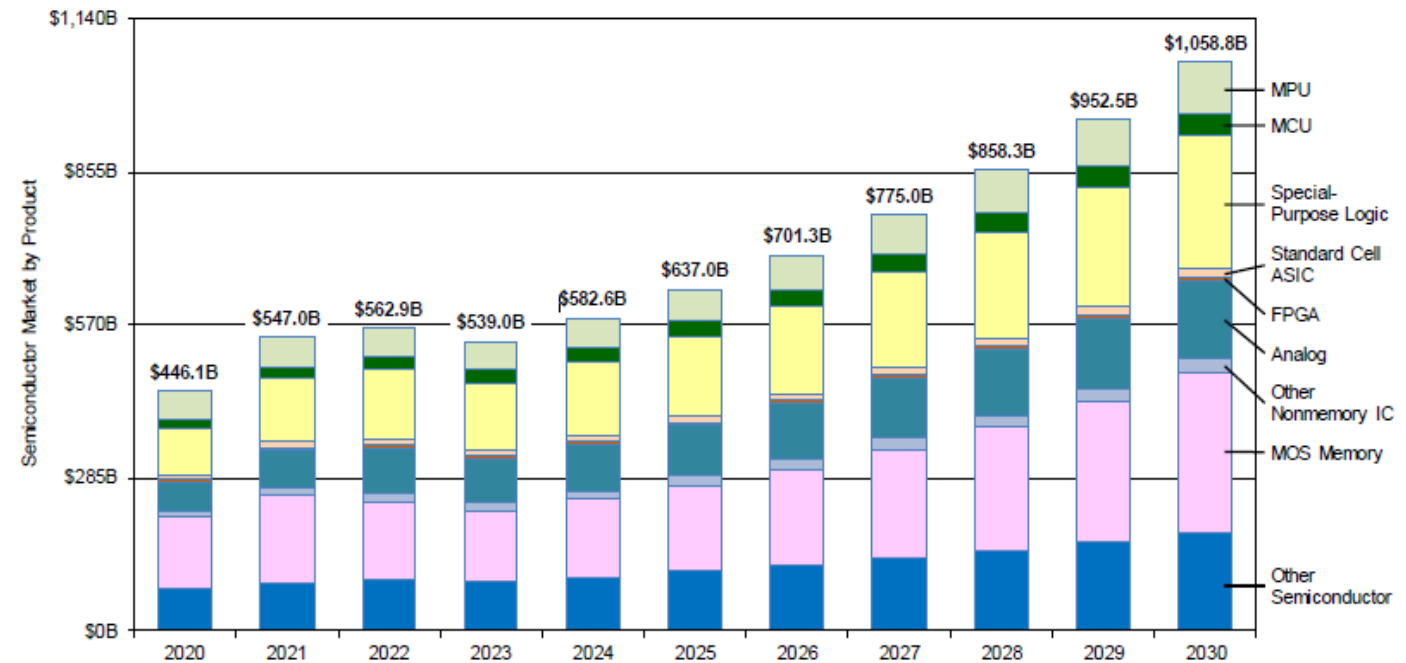
**Doubling of demand:**  
Market to exceed USD 1 Trillion before by 2030



**Emerging market opportunities:**  
AI, edge computing, digital transformation



**Technological change:**  
miniaturisation reaches its limits



(IBS, 2023)

**Digital Decade Target: Double EU share in global semiconductor production to 20% by 2030**

# The EU Chips Act

“ We will present a European Chips Act...  
This is not just a matter of our competitiveness.  
This is also a matter of **tech sovereignty**.  
Commission President Ursula von der Leyen

## Vision

To jointly create a **state-of-the-art** European chip ecosystem, that includes world-class **research**, **design** and **production** capacities

## Key objectives

- strengthen **research and technology** leadership
- build and reinforce its **innovation capacity** in design, manufacturing and packaging
- put in place framework to increase substantially **production capacity** by 2030
- address the acute **skills** shortage, attract new talent
- develop mechanism to monitor **supply chain** and intervene if needed

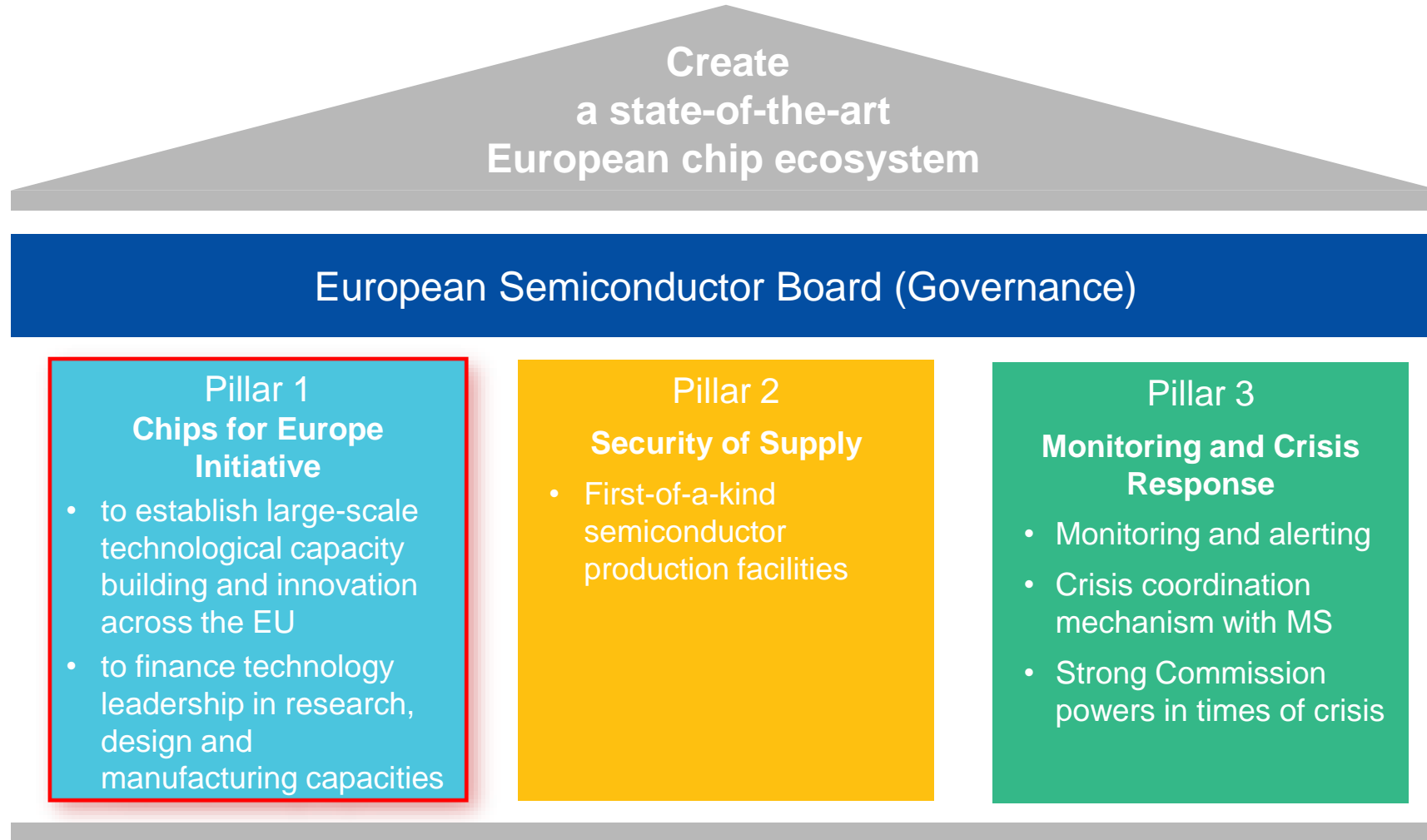


# EU Chips Act

- Context
- Pillar 1
  1. Design Platform
  2. Pilot Lines
  3. Quantum
  4. Competence Centres
  5. Chips Fund
- Pillar 2
- Pillar 3



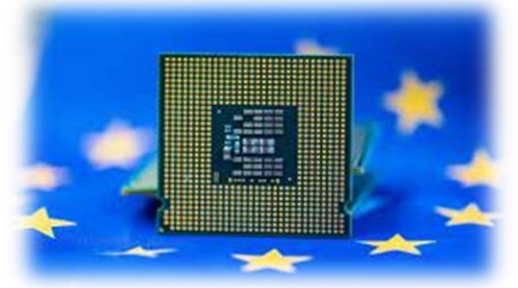
# Three pillars of the Chips Act



# Pillar 1

# Chips for Europe Initiative

## Rationale for the Initiative



### Situation today

- EU is strong in R&D, RTOs and in manufacturing equipment
- R&D supported by EU and Member States with ~4 B€ in MFF programmes

### What is the EU missing

- Capability for translating R&D excellence into new markets
- Industrial capabilities in leading-edge design and manufacturing
- Market pull



- EU + MS programmes cover R&D and innovation
- Measures to help **bridge the gap to market** are required

# Chips for Europe Initiative

Aim: bridging the gap from lab to fab

## 5 Objectives

- 1 Reinforce design capacity by providing a **virtual design platform**
- 2 Enhance existing and developing new **pilot lines**
- 3 Accelerate the development of **quantum chips**
- 4 Expand **skills** and set up a network of **competence centres**
- 5 Facilitate SME access to **equity and loans** through a dedicated **Chips Fund**

Chips JU

EIC  
I-EU

Basic  
Research

Applied  
Research

Prototyping

Pilot lines

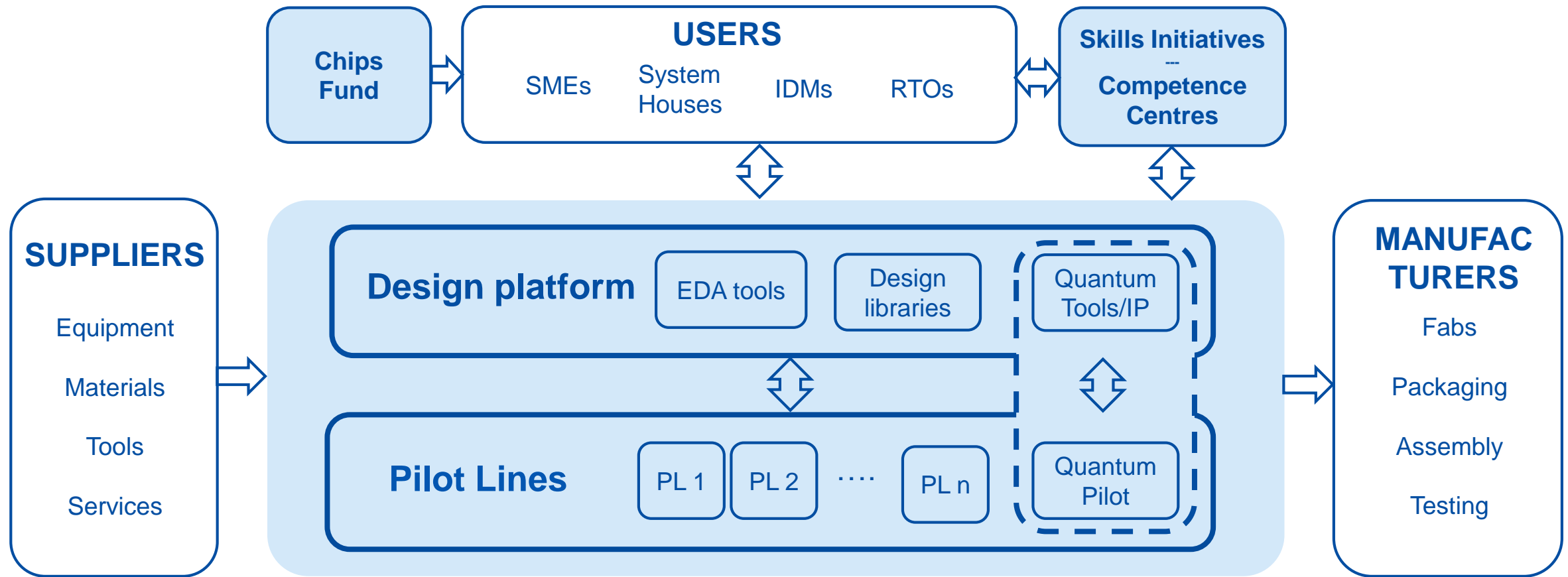
Production



European  
Commission

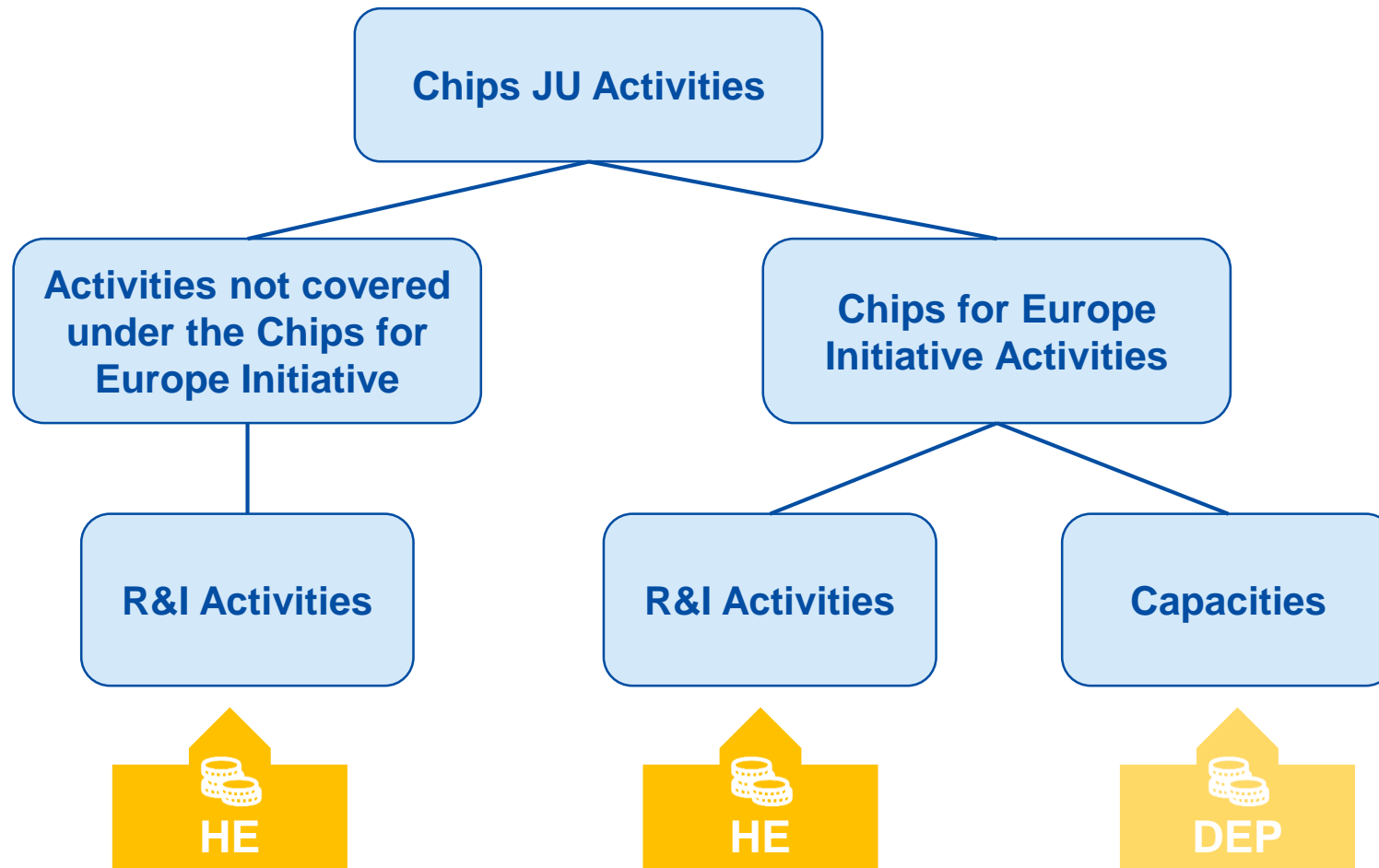
# Chips for Europe Initiative

## Bridging the gap from lab to fab



# Future “Chips JU” Activities

## Chips for Europe Initiative



Pillar 1

# 1- Design Platform

# Design platform - scope



## Ambition

Foster the development of the semiconductor **design ecosystem** in EU, reinforcing capacity to innovate and create European Intellectual Property through IC design

## Main scope

- **Reduce entry barriers** and administrative burden for EU companies engaging in chip design
- **Facilitate access** to pilot lines and manufacturing facilities
- Foster **collaboration** among EU stakeholders, also on new IP and tools (incl. open-source, quantum)
- **Access** to network of **competence centers** offering **training** and support to boost design skills

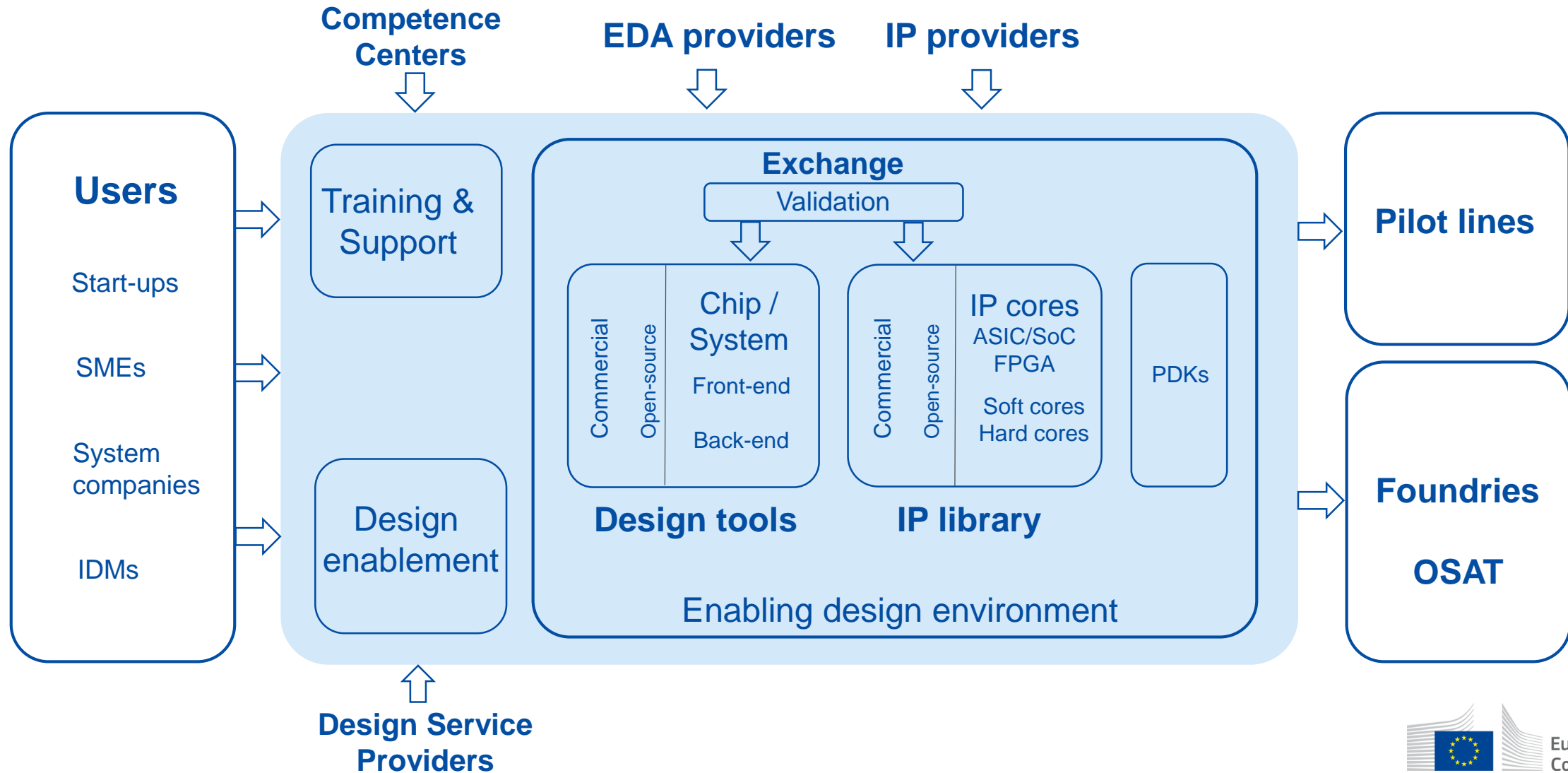


## Instrument



Develop a **virtual design platform**, offering **cloud-based** access to tools, libraries and support services to accelerate development and reduce time-to-market

# Design platform

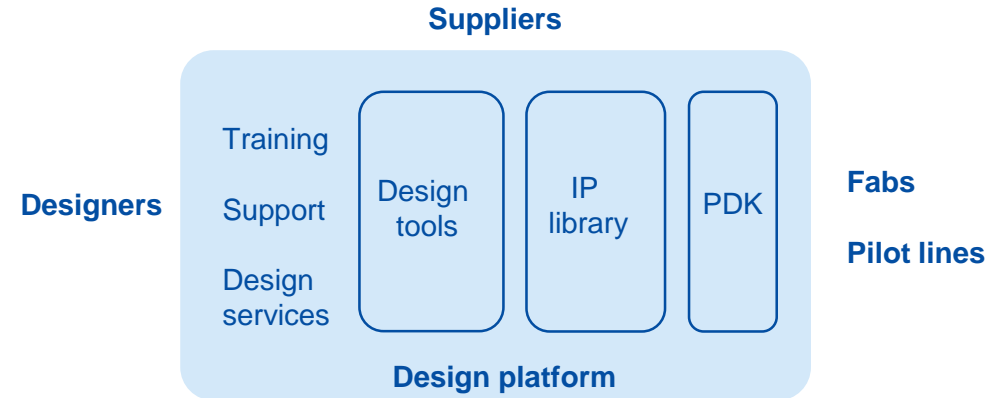


# Design platform Model

## Added value



- Easy access on the **cloud**
- No upfront CapEx for on-premise IT **infrastructure**
- Maximum computing **scalability** for simulation and verification
- High level of **security**, fully audited
- **Streamlined process** with framework agreements
- Access to **prototyping**, **MPW** and foundry services



## Key partners



- **Foundries**, **IP** vendors, **EDA** and **infrastructure** providers - collaboration for **secure cloud** solution
- **ASIC/SoC design services** for design enablement, workflows
- **Competence centers** offering training to address **skills** gap

# Pillar 1

## 2 - Pilot Lines

# Pilot Lines

## Semiconductors R&I challenges

EU semiconductor ecosystem: limited capability to convert **excellence in research** into **industrial innovation**

- Current **instruments** cannot provide a path for sustainable research **from the lab to industrialisation**
- We have **leading research organisations** but their outcomes are **not always taken up** by EU companies
- Chip development is **costly and risky**, particularly in early stages of new technologies
- Opportunities in **emerging trends** not always seized on time



**Pilot Lines** can be the response to these challenges

# Pilot Lines in the Chips Act



To enable development and deployment of cutting-edge and next generation semiconductor technologies

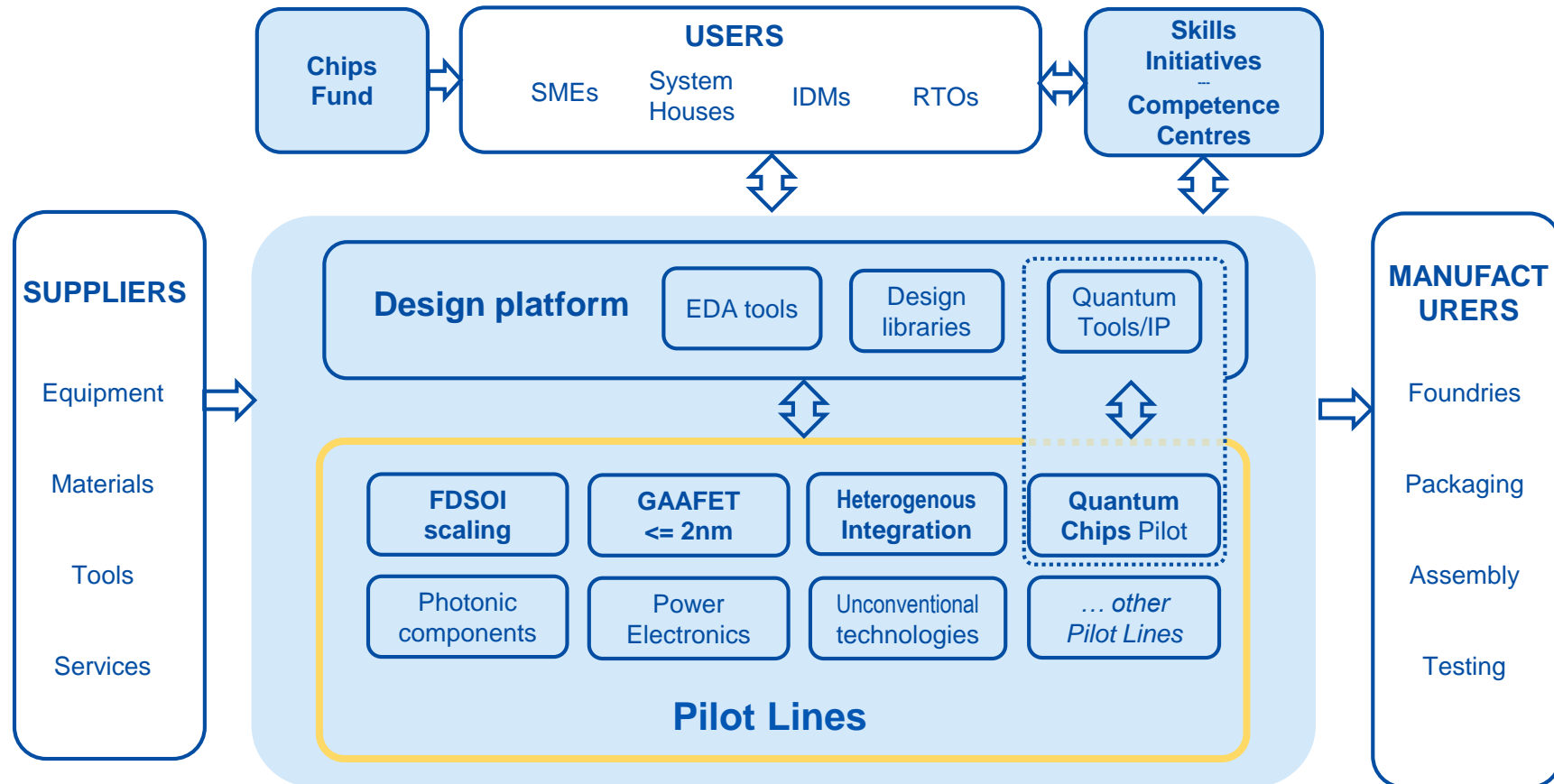
support enhancement of existing and development of new advanced pilot lines

To address structural challenges and market failures where such facilities are not available in the Union, hindering innovation potential and global competitiveness

investments from the Union, alongside with Member States and the private sector, in pilot lines is necessary

pilot lines should provide for the industry a facility to test, experiment and validate semiconductor technologies and system design concepts,

# Pilot Lines in the Chips Act



## Pilot Line Infrastructure

Central role:

- Scaled FD-SOI down to 10nm and below
- Leading-edge process at 2nm and below
- Advanced Het. System Integration

Other technologies:

- Quantum
- Photonic
- Power
- ...

# Pilot Lines



- **Key elements:** leading-edge, industrial relevance, user requirements, industrialization, pan-EU
- **Models:** From R&I to manufacturing, service provision, test and experimentation
- **Scope:** Microelectronics & Photonics, process technologies: front end, back end, system integration,..
- **Users:** Involvement, application/technology matching, support risk-taking
- **Access conditions:** Open, non discriminatory, cost efficient
- **Technology maturity:** TRL and MRL approaches
- **Skills:** contribution of pilot lines to on-the-job training, mobility of researchers
- Link to **Design Platform:** PDK, ADK, (virtual) prototyping, functional experimentation, validation...

# Implementation of Pilot Lines Timeline\*

## Phases

1. Consultations with hosting organisations (2Q2023)
2. Call for proposals (3Q2023)
3. Launch of first batch (1Q2024)

*\* Based on current estimation of the legislative process*

Pillar 1

# 4 – Competence Centre / Skills

# Skills in the Chips Act

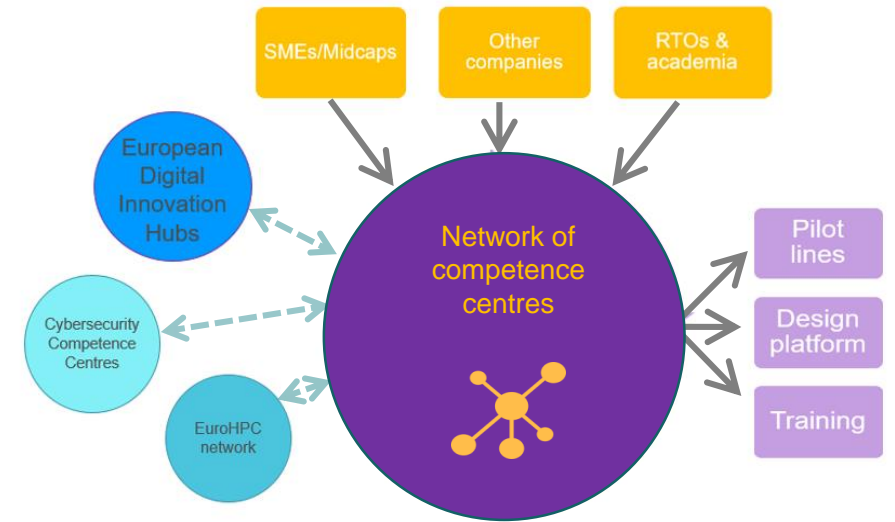


- **Chips JU** will have dedicated calls, in collaboration with Member States, for:
  - Public awareness campaigns
  - Scholarships and Traineeships
  - Free training, upskilling and reskilling programmes
  - Training and support programmes for SMEs
  - Link with complementary mobility under Erasmus+
- A **DEP call** on the above topics is already foreseen in Q3 2023
- Many actions will be coordinated by the **Competence Centres**

# EU Network of Competence centers

## Role of competence center

- Provide access to **training**, including upskilling and reskilling
- Facilitate access to **design platform** and **pilot lines**
- Support technology **transfer**
- Match **user needs** with available expertise in the network
- Act as reference for own area of **expertise**
- Raising **awareness** on international programmes, promoting **services**, **funding** opportunities



# EU Network of Competence centers



- Member States designate candidates
- Single organisation or coordinated group with complementary expertise
- Non profit organisation (RTOs, Uni's)
- Synergies with EDIHs, can become CCs
- Governance autonomy, in line with objectives of the Initiative



EU support for at least one centre per Member State



Co-investment with Member States and Regions



Supporting industry and public services



Access to design platform and pilot lines



Focus on Semiconductors Skills

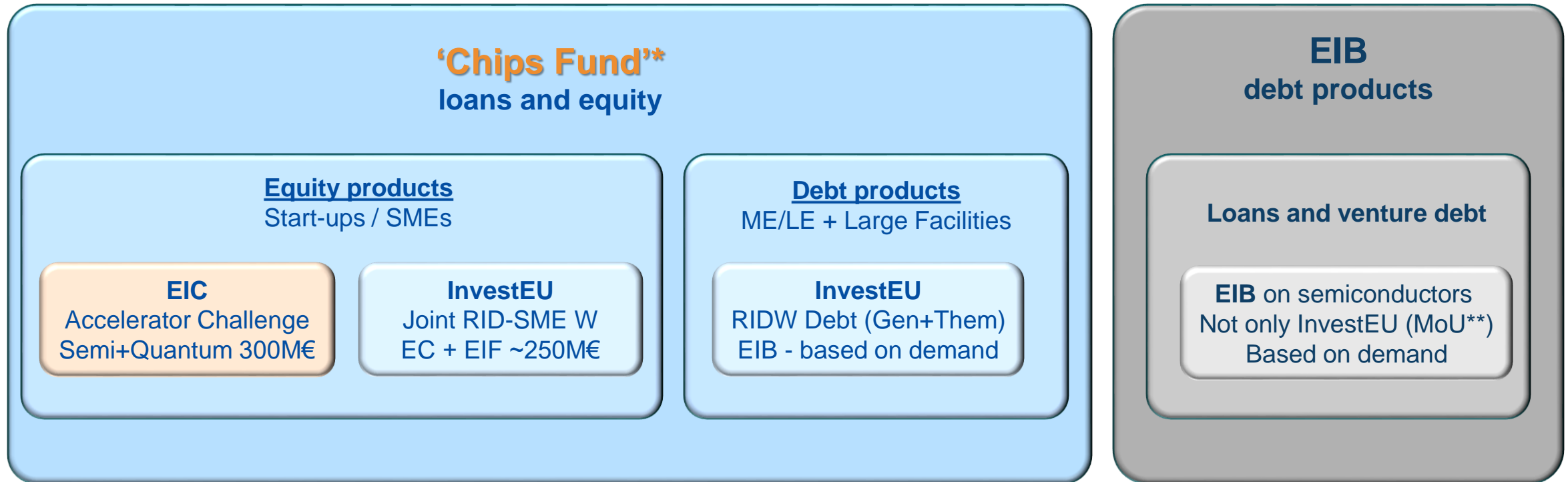


A strong European network of Competence Centres

# Pillar 1

## 5 – Chips Fund

# The “Chips fund” investment facility

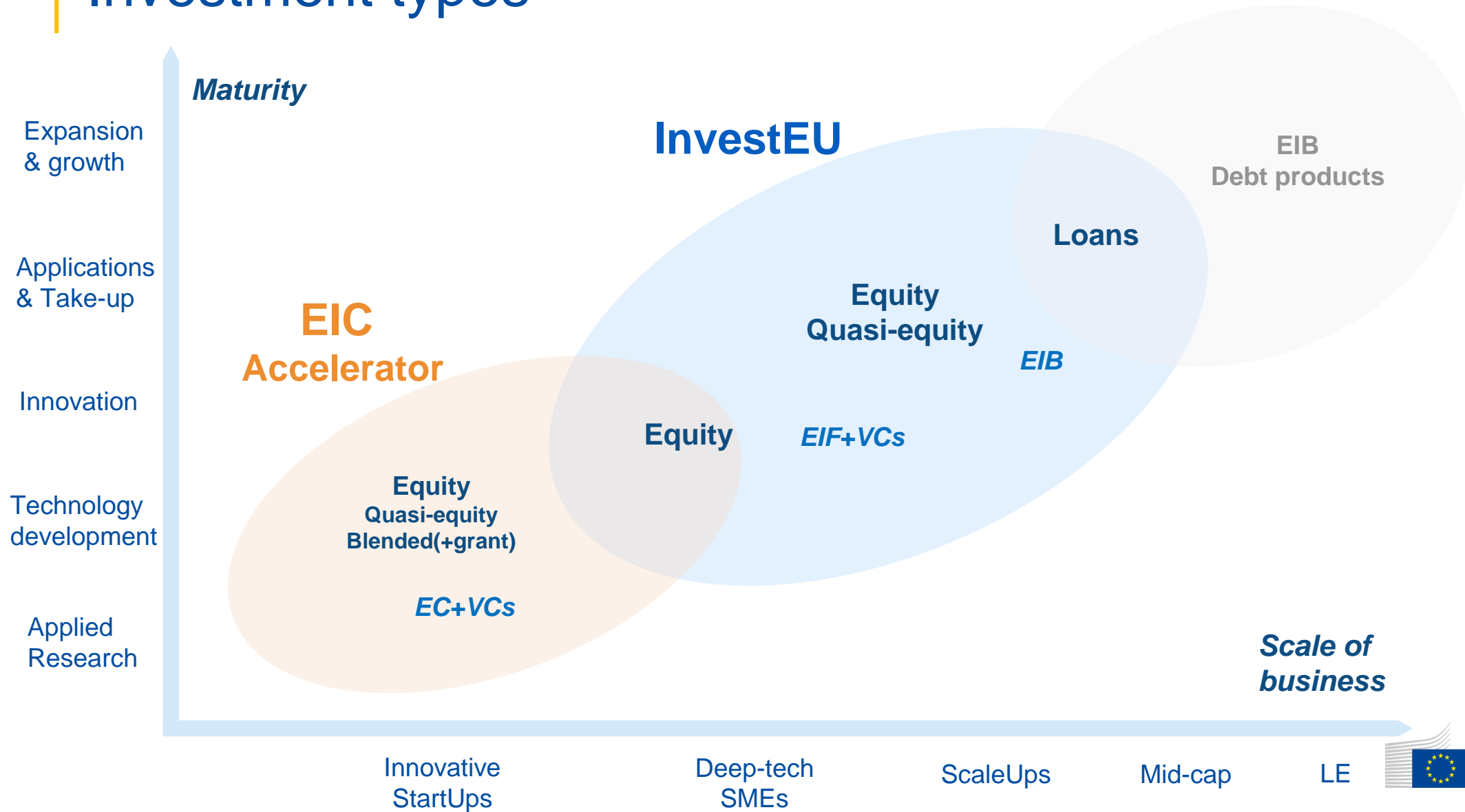


\* The “Chips Fund” will be implemented through an investment facility Fund and eligibility criteria are in current EIB group mandates

\*\* An MOU between EIB and EC for investments in semiconductors has been signed upon the Chips Act presentation (8/2/22)

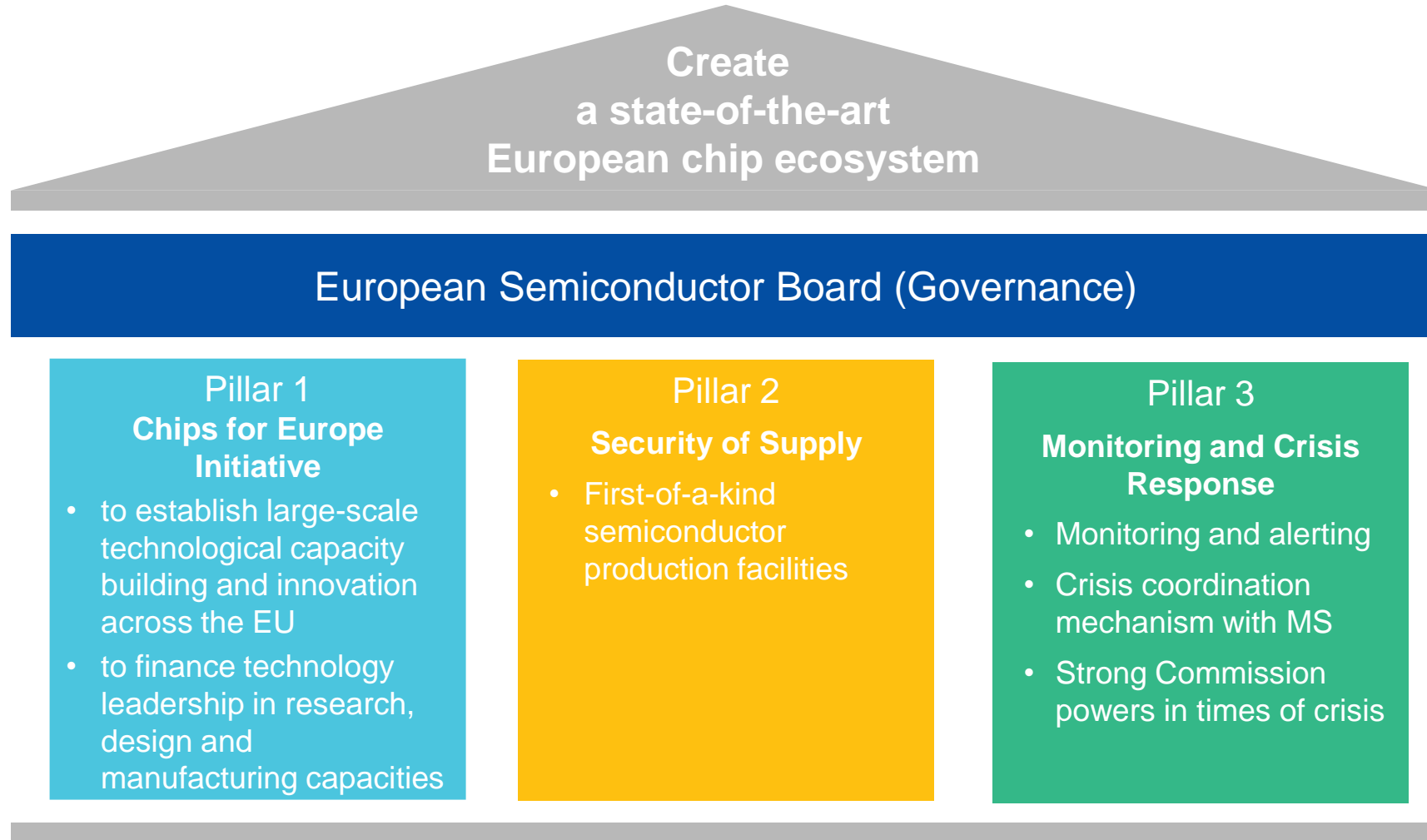
# Chips Fund

## Investment types



# Pillar 2

# Three pillars of the Chips Act



# Pillar 2 - Security of supply and resilience

## State aid for Manufacturing facilities

### Integrated Production Facility (IPF)

First-of-a-kind facility which produces the chips (mostly) for the same undertaking

### Open EU Foundry (OEF)

First-of-a-kind facility that produces chips (mostly) for unrelated undertakings



**First-of-a-kind facility:** to qualify, facility needs to offer innovation in terms of products or process that is not yet present in the Union (not to distort competition)



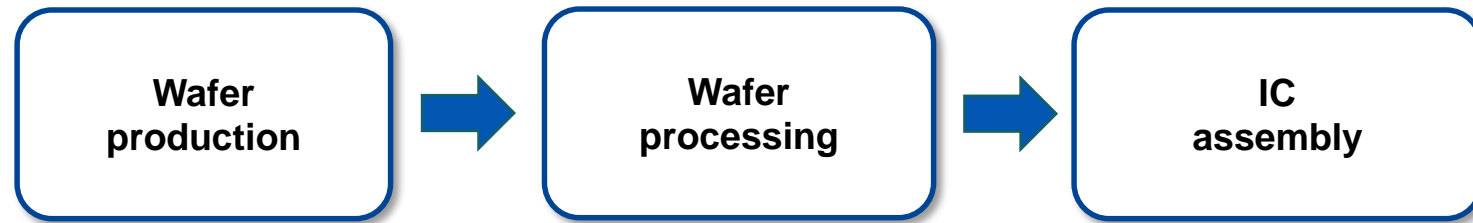
**Conditions:** positive impact, security of supply and commitment to next generation

*Relevant projects have been announced already by Intel, Infineon, ST-Microelectronics, GlobalFoundries...*

# Pillar 2 – Security of supply and resilience

## First of a Kind facilities: what qualifies

The main stages of semiconductor production may be eligible



Innovation can be in terms of:



technological performance

↘ ↙ *Not only*  
↗ ↖ *miniaturisation*



process innovation



energy and environmental performance

Parallel projects can be recognised as first-of-a-kind

# Pillar 3

# Pillar 3: Monitoring and crisis response

## Monitoring stage

- Regular monitoring by Member States and update mechanism for alerts by stakeholders
- Coordinated assessment of crisis response measures by Semiconductor Board



## Crisis trigger

When **assessment of Commission provides evidence** of serious disruptions in the supply

- entailing significant negative effects on one or more important sectors, or
- preventing the repair and maintenance of essential products used by critical sectors

## Commission implementing act

(preference for normal procedure, possibility for urgency procedure in exceptional cases)

## Crisis stage



- **Emergency Toolbox** activated: Information gathering, priority-rated orders, export control
- Intensified coordination in the Board

# Pillar 3: Monitoring and crisis response

## International partnerships

- Semiconductor value chain is global and spread over different world regions
- We need to cooperate with like-minded partner countries, proactively managing interdependencies to ensure
  - a reliable global marketplace for European products, and
  - security of supply, including in crisis situations

### EU-US Trade and Technology Council

- coordinate measures to secure supply of semiconductors
- joint actions to exchange information and to coordinate on:
  - Early warning systems to detect supply issues
  - Industry-led methods to estimate demand
  - avoid subsidy races
  - Improve understanding of global demand

Further: **Digital Partnerships** with Asian countries



# Chips Act – Process

**Commission** – Chips Act proposal in Feb 2022



## Council

- **Industry** CWP and **Research** CWP
- Adoption of General Approach Dec 2022



## Parliament

- 6 Parliamentary Committees involved, ITRE in the lead
- Plenary vote in Feb 2023



## Trilogue

Council-Parliament-Commission



**Chips Act  
Adoption**



# Thank you

## Q&A

**Marco Ceccarelli – EC DG CNECT**



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